In The Claims:

Please amend the claims as follows:

Claims 1-45 (canceled)

Claim 46 (previously presented) A method of forming a non-gate diode in a CMOS process, comprising:

providing a substrate having a well region therein;

forming a pair of blocking isolation structures in the substrate;

forming a first type doped region located in the well region and between the blocking isolation structures; and

forming a pair of second type doped regions located in the well region wherein the pair of second type doped regions are adjacent to the blocking isolation structure respectively and each second type doped region is separated from the first type doped region by the well.

Claim 47 (original) The method according to claim 46, wherein the first type doped region and the second type doped region are implanted with P-type and N-type ions respectively.

Claim 48 (original) The method according to claim 46, wherein the well region is lightly implanted with a P-type ion.

Claim 49 (previously presented) The method according to claim 46, wherein each second type doped region and the first type doped region defines a spacing, separating the second type doped region from the first type doped region.

Claim 50 (previously presented) The method according to claim 49, wherein the spacing is undoped.